SigmaTel, Inc.

Integrating Mixed-Signal Solutions

STAC9704/7

Multimedia Audio Codec for AC'97

GENERAL DESCRIPTION:

SigmaTel's **STAC9704/07** is a general purpose 18-bit, full duplex, audio codec that conforms to the analog component specification of AC'97 (Audio Codec '97 Component Specification rev. 1.03). The **STAC9704/07** incorporates ***SigmaTel's*** proprietary Sigma-Delta technology to achieve signal quality in excess of **95dB** SNR. The DACs, ADCs, and mixers are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, and 3 output channels. Also included are ***SigmaTel's*** 3D stereo enhancement (***SS3D***) and an extra true line-level out for headphones or speaker amplifiers. The **STAC9704/07** communicates via the five wire AC Link to any digital component of AC'97 providing flexibility in the audio system design. Packaged in a small AC'97 compliant 48-pin TQFP, the **STAC9704/07** can be placed on the motherboard, daughter boards, add-on cards, PCMCIA cards, or outside the main chassis such as in a speaker. The 9707 is identical to the 9704 except that the 9707 is tested at AVdd = DVdd = 3.3V.

FEATURES:

- **High performance ΣΔ technology**
- **18-bit full duplex stereo A/D, D/A**
- **AC-link protocol compliance**
- **Single power source from 5V to 3.3V**
- **AC'97 compliant mixer**
- ***SigmaTel Surround (SS3D)*** **Stereo Enhancement**
- **Energy saving power down modes**
- **48k sample/second rate**
- **Six analog line-level inputs**
- **48-pin TQFP**
- **SNR > 95 dB through Mixer and DAC**
- **STAC9707 is the 3.3 volt version**

ORDERING INFORMATION:

PART NUMBER	PACKAGE	TEMPERATURE RANGE	SUPPLY RANGE
STAC9704T	48-pin TQFP 7mm x 7mm x 1.4mm	0^{O} C to $+70^{O}$ C	DVdd = 3.3V – 5V, AVdd = 5V
STAC9707T	48-pin TQFP 7mm x 7mm x 1.4mm	0^{O} C to $+70^{O}$ C	DVdd = 3.3V AVdd = 3.3V

SigmaTel reserves the right to change specifications without notice.

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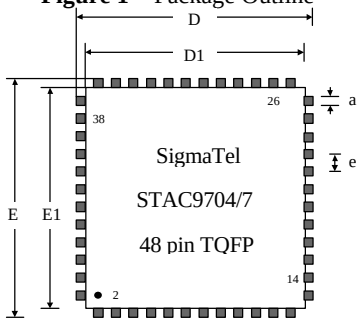


Table 1 - Package Dimensions

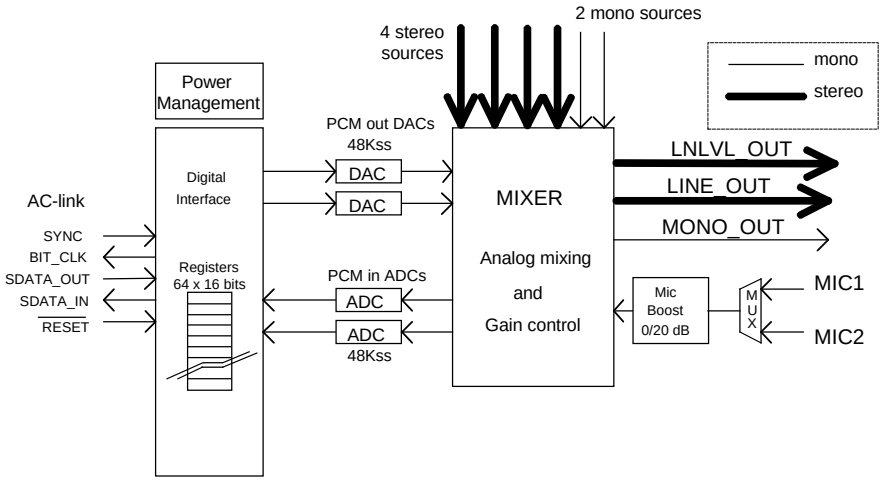
KEY	9704/7 DIMENSION TQFP
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

Table 2 - Pin Designation

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
1	DVdd1	*13*	PHONE	*25*	AVdd1	*37*	MONO_OUT
2	XTL_IN	*14*	AUX_L	*26*	AVss1	*38*	AVdd2
3	XTL_OUT	*15*	AUX_R	*27*	Vref	*39*	LNLVL_OUT_L
4	DVss1	*16*	VIDEO_L	*28*	Vrefout	*40*	NC
5	SDATA_OUT	*17*	VIDEO_R	*29*	AFILT1	*41*	LNLVL_OUT_R
6	BIT_CLK	*18*	CD_L	*30*	AFILT2	*42*	AVss2
7	DVss2	*19*	CD_GND	*31*	NC	*43*	NC
8	SDATA_IN	*20*	CD_R	*32*	CAP2	*44*	NC
9	DVdd2	*21*	MIC1	*33*	NC	*45*	NC
10	SYNC	*22*	MIC2	*34*	NC	*46*	NC
11	RESET#	*23*	LINE_IN_L	*35*	LINE_OUT_L	*47*	NC
12	PC_BEEP	*24*	LINE_IN_R	*36*	LINE_OUT_R	*48*	NC

# denotes active low

Figure 2. **STAC9704** Block Diagram

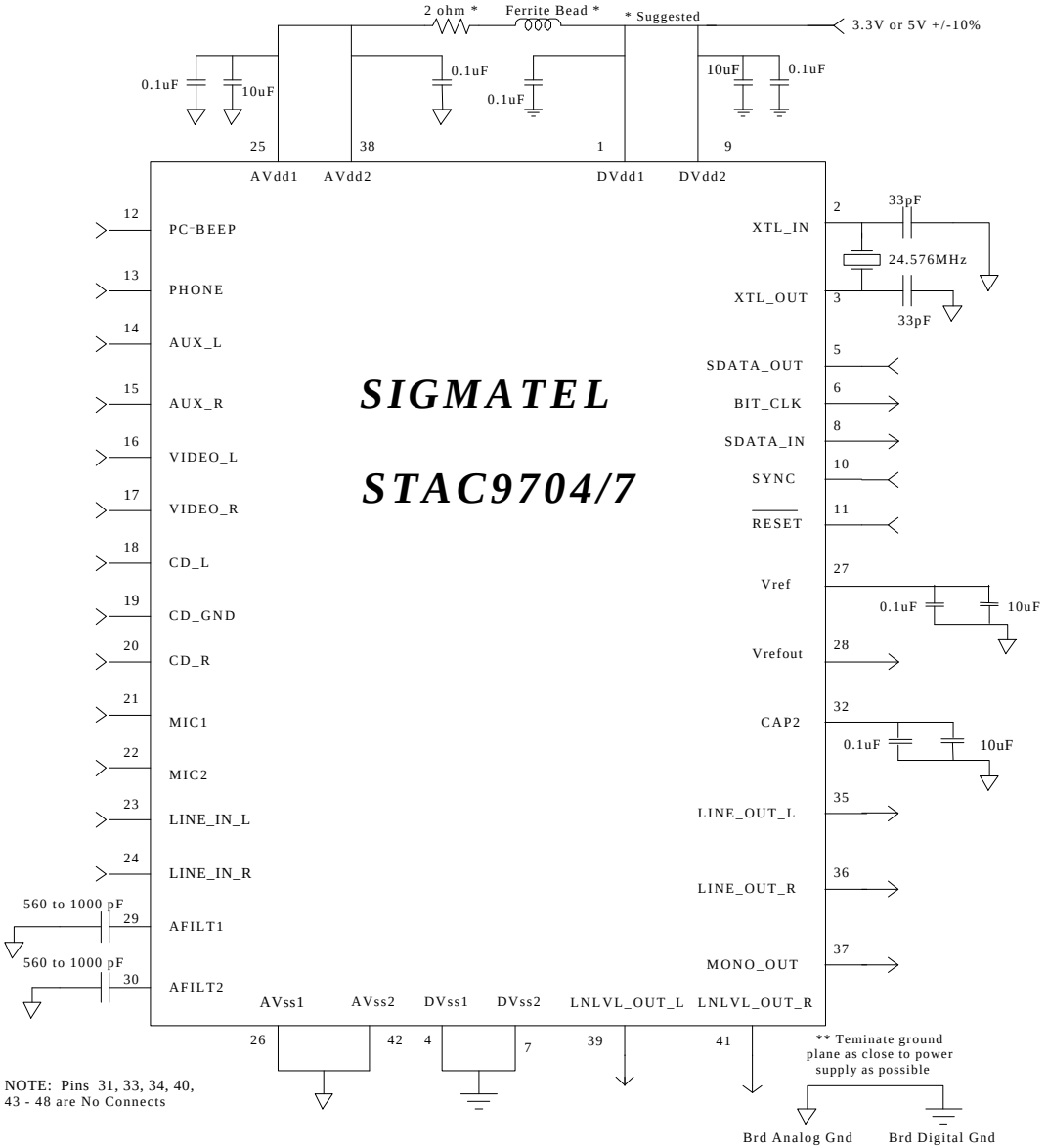


The **STAC9704/7** block diagram, above, illustrates its primary functional blocks. It performs fixed 48K sample rate D-A & A-D conversion, mixing, and analog processing. The digital interface communicates with the AC'97 controller via the five wire AC-link and contains the 64 word by 16-bit registers. Two fixed 48Kss DAC's support a stereo PCM-out channel which contains a mix generated in the AC'97 controller of all software sources, including the internal synthesizer and any other digital sources. The Mixer block mixes the PCM-out with any analog sources, then outputs to LINE_OUT and LNLVL_OUT. The MONO_OUT delivers either mic only or a mono mix of sources from the mixer. The two fixed 48Ks ADC's take any mix of mono or stereo sources, and convert it to a stereo PCM-in signal. All ADCs and DACs operate at 18-bit resolution.

The **STAC9704/7** is designed primarily to support stereo, 2-speaker PC audio. However, multi-channel encoded stereo can be played out through the LINE_OUT and LNLVL_OUT. This encoded signal can be played on normal stereo speakers, or sent to consumer equipment or other decoding devices via LINE_OUT and LNLVL_OUT to an analog input connection for multi-channel playback. As an option, the **STAC9704/07** provides for a stereo enhancement feature, ***Sigmatel Surround 3D (SS3D).*** ***SS3D*** provides the listener with several options to expand the soundstage beyond the normal 2-speaker arrangement.

Together with the logic component (controller) of AC'97, **STAC9704/7** can be SoundBlaster® and Windows® Sound System compatible. SoundBlaster® is a registered trademark of Creative Labs. Windows® is a registered trademark of Microsoft Corporation.

Figure 3 - Connection Diagram –
See Appendix A for an alternative connection diagram when using separate supplies.
See Appendix B for specific connection requirements prior to operation.



1. PIN/SIGNAL DESCRIPTIONS

1.1 Digital I/O

These signals connect the **STAC9704/7** to its AC'97 controller counterpart and an external crystal.

Table 3. Digital Signal List

SIGNAL NAME	TYPE	DESCRIPTION
RESET #	I	AC'97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 kHz fixed rate sample sync
BIT_CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC'97 input stream
SDATA__IN	O	Serial, time division multiplexed, AC'97 output stream

# denotes active low

1.2 Analog I/O

These signals connect the **STAC9704/7** to analog sources and sinks, including microphones and speakers.

Table 4. Analog Signal List

SIGNAL NAME	TYPE	DESCRIPTION
PC-BEEP	I	PC Speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE-IN-L	I	Line In Left Channel
LINE-IN-R	I	Line In Right Channel
CD-L	I	CD Audio Left Channel
CD-GND	I	CD Audio analog ground
CD-R	I	CD Audio Right Channel
VIDEO-L	I	Video Audio Left Channel
VIDEO-R	I	Video Audio Right Channel
AUX-L	I	Aux Left Channel
AUX-R	I	Aux Right Channel
LINE-OUT-L	O	Line Out Left Channel
LINE-OUT-R	O	Line Out Right Channel
MONO-OUT	O	To telephony subsystem speakerphone (or DLP – Down Line Phone)

LNLVL_OUT_L	O	True Line Level Out Left Channel
LNLVL_OUT_R	O	True Line Level Out Right Channel

* Note: any unused input pins should have a capacitor (1 uF suggested) to ground.

1.3 Filter and Voltage References

These signals are connected to resistors, capacitors, or specific voltages.

Table 5. Filtering and Voltage References

SIGNAL NAME	TYPE	DESCRIPTION
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFILT2	O	Anti-Aliasing Filter Cap - ADC channel
CAP2	O	ADC reference Cap

1.4 Power and Ground Signals

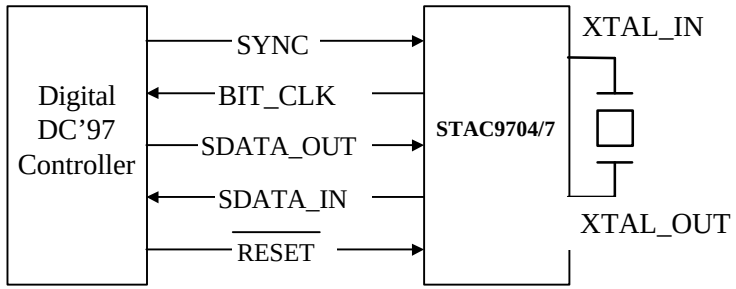
Table 6. Power Signal List **STAC9704/7**

SIGNAL NAME	TYPE	STAC9704	STAC9707
AVdd1	I	Analog Vdd = 5.0V	Analog Vdd = 3.3V
AVdd2	I	Analog Vdd = 5.0V	Analog Vdd = 3.3V
AVss1	I	Analog Gnd	Analog Gnd
AVss2	I	Analog Gnd	Analog Gnd
DVdd1	I	Digital Vdd = 5.0V or 3.3V	Digital Vdd = 3.3V
DVdd2	I	Digital Vdd = 5.0V or 3.3V	Digital Vdd = 3.3V
DVss1	I	Digital Gnd	Digital Gnd
DVss2	I	Digital Gnd	Digital Gnd

2. AC-LINK

Below is the figure of the AC-link point to point serial interconnect between the **STAC9704/7** and its companion controller. All digital audio streams and command/status information are communicated over this AC-link. Please refer to the "Digital Interface" section 3 for details.

Figure 4. **STAC9704/7'**s AC97-link to its companion controller



2.1 Clocking

STAC9704/7 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz (half of crystal frequency).

The beginning of all audio sample packets, or "Audio Frames", transferred over AC-link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

2.2 Reset

There are 3 types of resets as detailed under "Timing Characteristics".

1. a "cold" reset where all **STAC9704/7** logic and registers are initialized to their default state
2. a "warm" reset where the contents of the **STAC9704/7** register set are left unaltered
3. a "register" reset which only initializes the **STAC9704/7** registers to their default states

After signaling a reset to the **STAC9704/7,** the AC'97 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication via register 26h from the **STAC9704/7.**

For proper reset operation, SDATA_OUT should be "0" during "cold" reset.

3. DIGITAL INTERFACE

3.1 AC-link Digital Serial Interface Protocol

The **STAC9704/7** communicates to the AC'97 controller via a 5 pin digital serial interface called AC-link, which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point to point serial interconnect. This link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-link data transaction. The following data streams are available on the **STAC9704/7:**

- **PCM Playback** **2 output slots** 2 Channel composite PCM output stream
- **PCM Record data** **2 input slots** 2 Channel composite PCM input stream
- **Control** **2 output slots** Control register write port
- **Status** **2 input slots** Control register read port

Synchronization of all AC-link data transactions is signaled by the AC'97 controller. The **STAC9704/7** drives the serial bit clock onto AC-link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

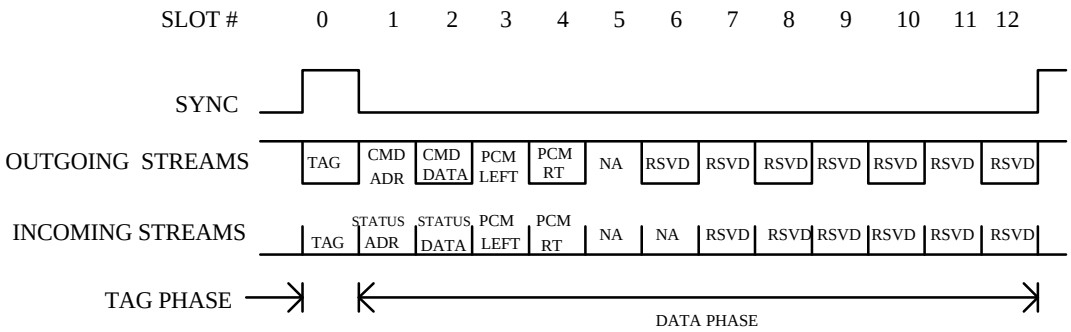
SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, **STAC9704/7** for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit (13-bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, it is the responsibility of the source of the data, (**STAC9704/7** for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted.

Figure 5. AC'97 Standard Bi-directional Audio Frame

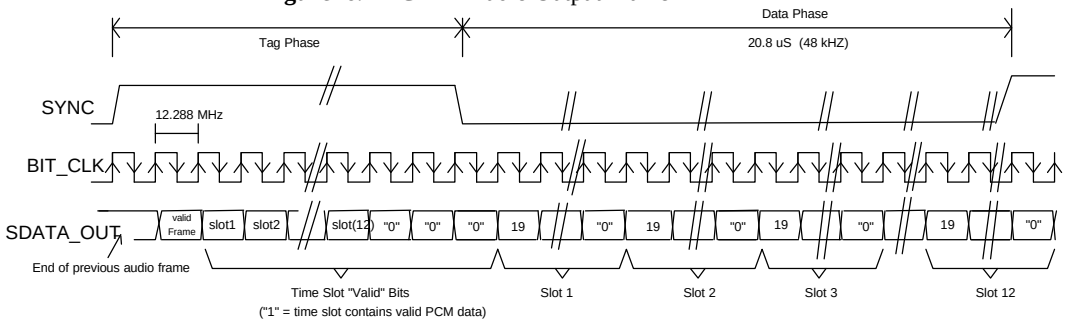


3.1.1 AC-link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the **STAC9704/7** DAC inputs, and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-link protocol infrastructure.

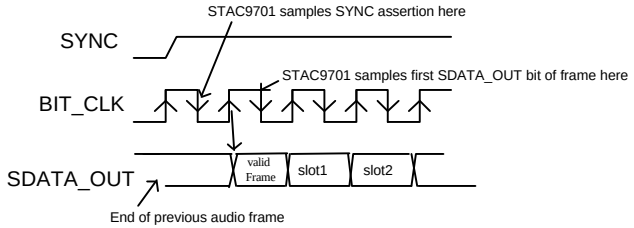
Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the **STAC9704/7** indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. The following diagram illustrates the time slot based AC-link protocol.

Figure 6. AC-link Audio Output Frame



A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the **STAC9704/7** samples the assertion of SYNC. This following edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the **STAC9704/7** on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 7: Start of an Audio Output Frame



SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC'97 controller When mono audio sample streams are sent from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

3.1.1.1 Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) of the **STAC9704/7** functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Audio output frame slot 1 communicates control register address, and write/read command information to the **STAC9704/7**.

Command Address Port bit assignments:

Bit (19) Read/Write command (1= read, 0=write)
Bit (18:12) Control Register Index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0) Reserved (Stuffed with 0's)

The first bit (MSB) sampled by **STAC9704/7** indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must he stuffed with 0's by the AC'97 controller.

3.1.1.2 Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit (19:4)	Control Register Write Data	(Stuffed with 0's if current operation is a read)
Bit (3 :0)	Reserved	(Stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC'97 controller.

3.1.1.3 Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

3.1.1.4 Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

3.1.1.5 Slots 5-12: Reserved

Audio output frame slots 5-12 are reserved for future use and are always stuffed with 0's by the AC'97 controller.

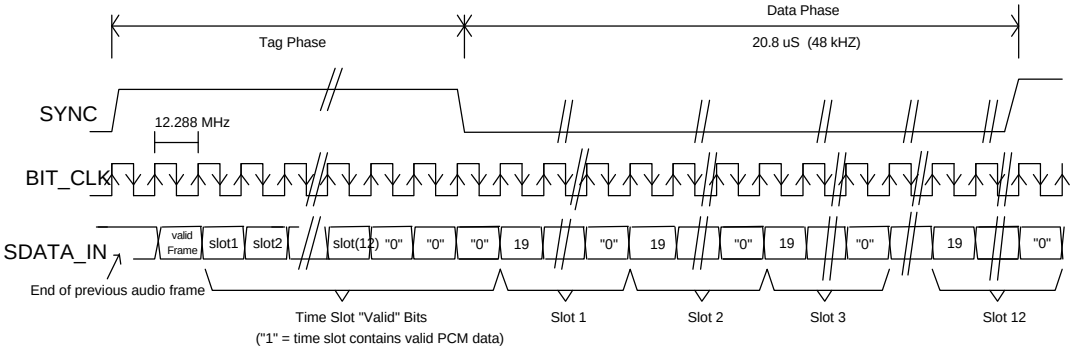
3.1.2 AC-link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the **STAC9704/7** is in the "Codec Ready" state or not. If the “Codec Ready” bit is a 0, this indicates that **STAC9704/7** is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while **STAC9704/7**’s voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1, it indicates that the AC-link and **STAC9704/7** control/status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

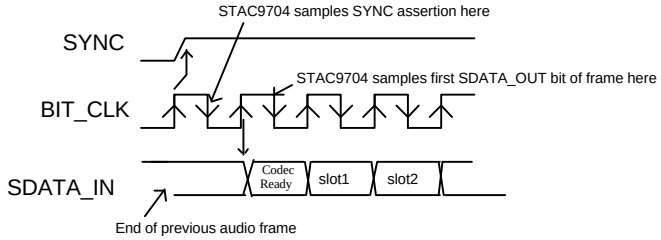
Prior to any attempts at putting **STAC9704/7** into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that **STAC9704/7** has become "Codec Ready". Once the **STAC9704/7** is sampled "Codec Ready", the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-link protocol.

Figure 8: **STAC9704/7** Audio Input Frame



A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, **STAC9704/7** samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the **STAC9704/7** transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 9: Start of an Audio Input Frame



SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by **STAC9704/7**. SDATA_IN data is sampled on the falling edges of BIT_CLK.

3.1.2.1 Slot 1: Status Address Port

The status port is used to monitor status for **STAC9704/7** functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by **STAC9704/7** during slot 0)

Status Address Port hit assignments:

Bit (19)	RESERVED	(Stuffed with 0)
Bit (18;12)	Control Register Index	(Echo of register index for which data is being returned)
Bit (11:0)	RESERVED	(Stuffed with 0's)

The first bit (MSB) generated by **STAC9704/7** is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0's by **STAC9704/7**.

3.1.2.2 Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control Register Read Data	(Stuffed with 0's if tagged "invalid")
Bit (3 :0)	RESERVED	(Stuffed with 0's)

If Slot 2 is tagged "invalid" by **STAC9704/7,** then the entire slot will be stuffed with 0's.

3.1.2.3 Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of **STAC9704/7** input MUX, post-ADC. **STAC9704/7** ADCs are implemented to support 18-bit resolution.

STAC9704/7 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

3.1.2.4 Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of **STAC9704/7** input MUX, post-ADC.

STAC9704/7 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

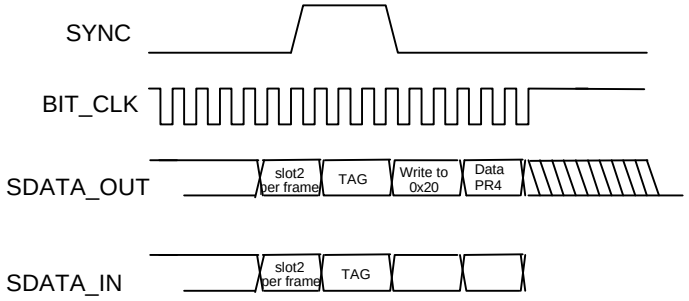
3.1.2.5 Slots 5-12: Reserved

Audio input frame slots 5-12 are reserved for future use and are always stuffed with 0's.

3.2 AC-link Low Power Mode

The **STAC9704/7's** AC-Link can be placed in the low power mode by programming Register 26h to the appropriate value. SDATA_IN is held at a logic low voltage level. The BIT_CLK is held at logic high after slot 2, in violation of the AC97 specification. This issue is detailed in the STAC9704 errata, and has not caused customer problems. The AC'97 controller can wake up the **STAC9704/7** by providing the appropriate reset signals.

Figure 10. **STAC9704/7** Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC, and SDATA_OUT low after programming the **STAC9704/7** to this low power mode.

3.2.1 Waking up the AC-link

Once the **STAC9704/7** has halted BIT_CLK, there are only two ways to "wake up" the AC-link. Both methods must be activated by the AC'97 controller. The AC-link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers will keep their current state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_IN will be activated, or re-activated as the case may be, and all **STAC9704/7** control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input. # denotes active low

Warm Reset - a warm reset will re-activate the AC-link without altering the current **STAC9704/7** register values. A warm reset is signaled by driving SYNC high for a minimum of 1 us in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the **STAC9704/7**.

4. STAC9704/7 MIXER

The **STAC9704/7** mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. These include:

- **System Audio**: digital PCM input and output for business, games and multimedia
- **CD/DVD**: analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop mic, with programmable boost and gain
- **Speakerphone**: use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

Figure 11. **STAC9704/7** Mixer Functional Diagram

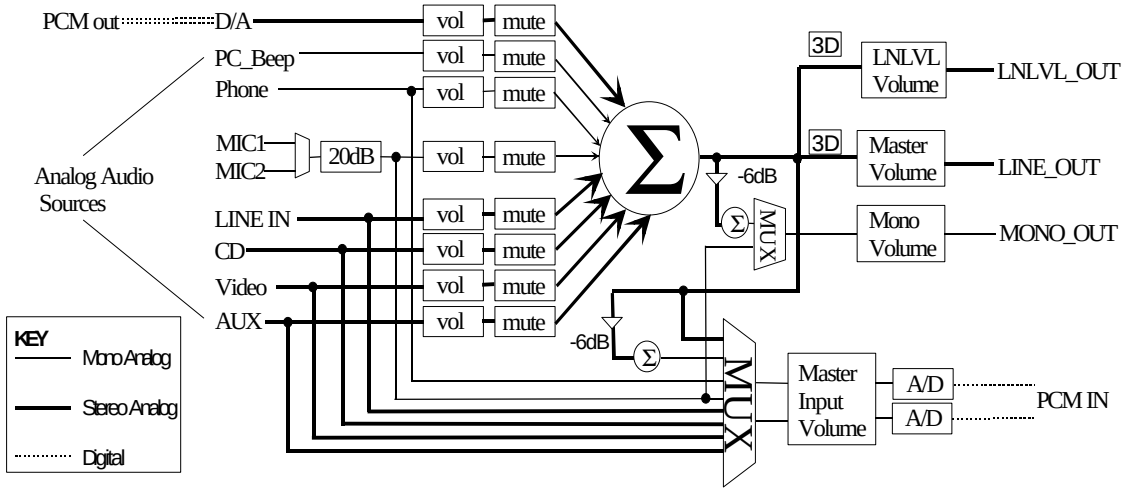


Table 8. Mixer functional connections

SOURCE	FUNCTION	CONNECTION
PC_Beep	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC'97 Controller	AC-link
LINE_OUT	stereo mix of all sources	To output jack
LNLVL_OUT	Additional stereo mix of all sources	To output jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital audio input to AC'97 Controller	AC-link

4.1 Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The **STAC9704/7** supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

Note: any unused input pins must have a capacitor (1 uF suggested) to ground.

4.2 Mixer Output

The mixer generates two distinct outputs:

- a stereo mix of all sources for output to the LINE_OUT
- a stereo mix of all sources for output to the LNLVL_OUT
- a mono, mic only or mix of all sources for MONO_OUT

  * Note: Mono output of stereo mix is attenuated by 6 dB.

4.3 PC Beep Implementation

PC Beep is active on power up and defaults to an unmuted state. During active RESET#, PC_BEEP is passed through the codec to LINE_OUT. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

4.4 Mixer Registers:

Table 9. Mixer Registers

REG #	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE FAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	NA
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	X	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DP1	DP0	0000h
26h	Powerdown Ctrl/Stat	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	NA
7Eh	Vendor ID2	0	1	1	1	0	1	1	0	0	0	0	0	0	1	0	0	NA

Notes:

1. All registers not shown and bits containing an X are reserved.

2. Any reserved bits, marked X, can be written to but are don't care upon read back.

3. PC_BEEP default to 0000h, mute off.

4. If optional bits D13, D5 of register 02H or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 3Fh as a value for this attenuation/gain block.

4.4.1 Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.

4.4.2 Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), register 04h controls the optional stereo true line level out, and register 06h controls the mono volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

Table 10: Play Master Volume Register

MUTE	Mx5…Mx0	FUNCTION	RANGE
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

4.4.3 PC Beep Register (Index 0Ah)

This register controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the **STAC9704/7** mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. NOTE: the PC_BEEP is recommended to be routed to L & R Line outputs even when the **STAC9704/7** is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

Table 11: PC_BEEP Register

MUTE	PV3…PV0	FUNCTION
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

4.4.4 Analog Mixer Input Gain Registers (Index 0Ch - 18h)

These registers control the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. Register 0Eh (Mic Volume Register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1, the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on. The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

Table 12: Analog Mixer Input Gain Register

MUTE	Gx4…Gx0	FUNCTION
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	-∞ dB gain

4.4.5 Record Select Control Register (Index 1Ah)

Used to select the record source independently for right and left. The default value is 0000h, which corresponds to Mic in.

Table 13: Record Select Control Registers

SR2…SR0	RIGHT RECORD SOURCE
0	Mic
1	CD In (right)
2	Video In (right)
3	Aux In (right)
4	Line In (right)
5	Stereo Mix (right)
6	Mono Mix
7	Phone

SL2…SL0	LEFT RECORD SOURCE
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

4.4.6 Record Gain Registers (Index 1Ch)

The 1Ch register adjusts stereo input record gain. Each step corresponds to 1.5 dB. 22.5 dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Table 14: Record Gain Registers

MUTE	GX3… GX0	FUNCTION
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

4.4.7 General Purpose Register (Index 20h)

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the mic selector. The LPBK bit enables loopback of the ADC output to the DAC input, without involving the AC-link, allowing for full system performance measurements.

Table 15: General Purpose Register

BIT	FUNCTION
3D	3D Stereo Enhancement on/off 1 = on
MIX	Mono output select 0 = Mix, 1= Mic
MS	Mic select 0 = Mic1, 1 = Mic2
LPBK	ADC/DAC loopback mode

4.4.8 3D Control Register (Index 22h)

This register is used to control the 3D stereo enhancement function, ***Sigmatel Surround 3D (SS3D),*** built into the AC'97 component. Note the register bits, DP1 – DP0, are used to control the separation ratios in the 3D control. ***SS3D*** provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality and for the bits in 22h to take effect.

Table 16: 3D Control Registers

DP1 – DP0	SEPARATION RATIO
0 0	3 (Default)
0 1	3 (Low)
1 0	4.5 (Med.)
1 1	6 (High)

3 separation ratios are implemented as shown above. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide for options to narrow or widen the soundstage.

4.4.9 Powerdown Control/Status Register (Index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsection is "ready". *Ready* is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready.

Table 17: Powerdown Status Register

BIT	FUNCTION
REF	VREF's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

5. LOW POWER MODES

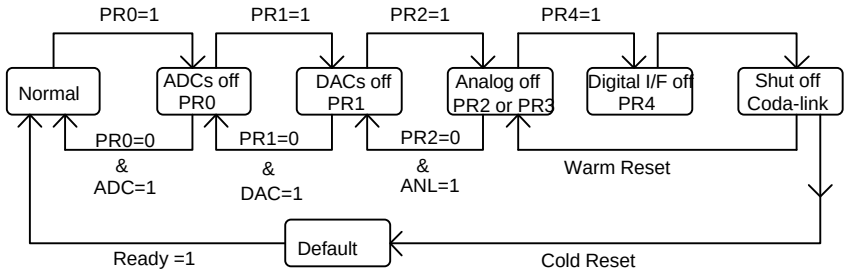
The **STAC9704/7** is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 18. The first three bits , PR0..PR2, can be used individually or in combination with each other, and control power distribution to the ADC's, DAC's and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR1, PR2, and PR3. PR3 essentially removes power from all analog sections of the codec, and is generally only asserted when the codec will not be needed for long periods. PR0 and PR1 control the PCM ADC's and DAC's only. PR2 and PR3 do not need to be "set" before a PR4, but PR0 and PR1 must be "set" before PR4.

Table 18: Low Power Modes

GRP BITS	FUNCTION
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (extnl clk off)
PR5	Internal Clk disable

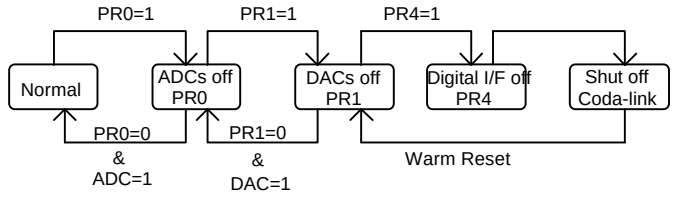
PR6	Not implemented

Figure 12: Example of **STAC9704/7** Powerdown/Powerup flow



The above figure illustrates one example procedure to do a complete powerdown of **STAC9704/7**. From normal operation, sequential writes to the Powerdown Register are performed to power down **STAC9704/7** a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-link (resetting PR4 to zero). The **STAC9704/7** can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

Figure 13: STAC9704/7 Powerdown/Powerup flow with analog still alive



The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through **STAC9704/7** to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

6. TESTABILITY

The **STAC9704/7** has two test modes. One is for ATE in-circuit test and the other is restricted for ***SigmaTel's*** internal use. **STAC9704/7** enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the **STAC9704/7** must be issued another rest with all AC-link signals held low to return to the normal operating mode.

7. AC TIMING CHARACTERISTICS

($T_{ambient}$ = 25° C, AVdd = DVdd = 5.0V or 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

7.1 Cold Reset

Figure 14: Cold Reset

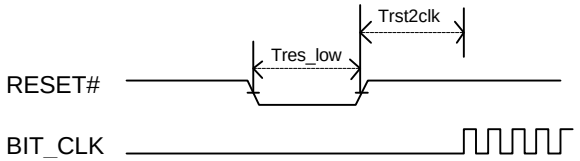


Table 19 : Cold Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

# denotes active low.

7.2 Warm Reset

As per the STAC9704 errata, the BIT_CLK is triggered on the rising edge of the SYNC pulse rather than the falling edge of the SYNC pulse as specified in the AC97 specification. This issue is not known to have caused any customer problems.

Figure 15: Warm Reset

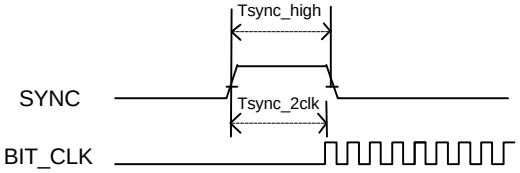


Table 20: Warm Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYNC active high pulse width	Tsync_high	-	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync_2clk	162.8	-	-	ns

7.3 Clocks

Figure 16: Clocks

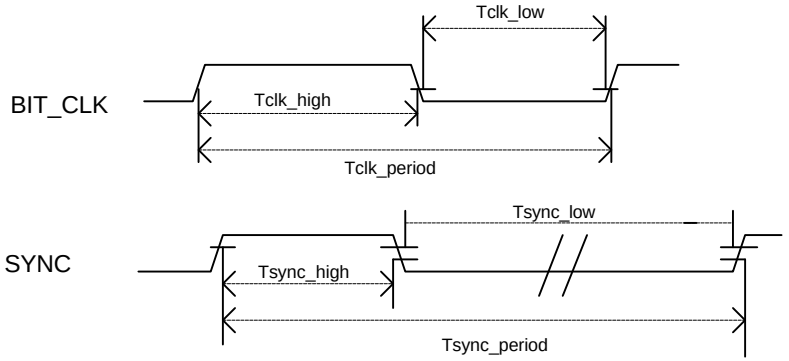


Table 21: Clocks

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BLT_CLK high pulsewidth (note 1)	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK low pulse width (note 1)	Tclk_low	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Notes: 1) Worst case duty cycle restricted to 40/60.

7.4 Data Setup and Hold (50pF external load)

Figure 17: Data Setup and Hold

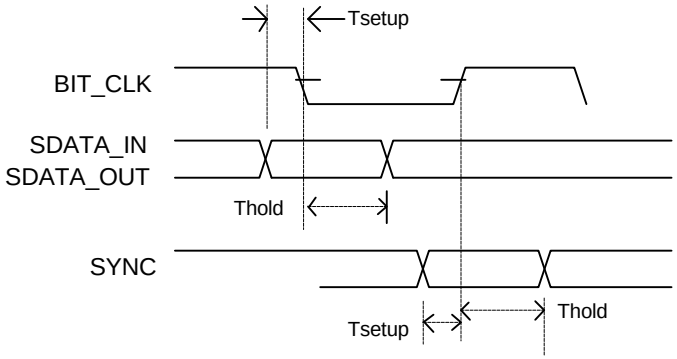


Table 22: Data Setup and Hold

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to falling edge of BIT_CLK	Tsetup	15.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	5.0	-	-	ns

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

7.5 Signal Rise and Fall Times - (50pF external load; from 10% to 90% of Vdd)

Figure 18: Signal Rise and Fall Times

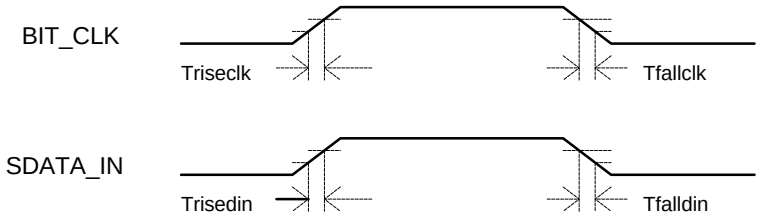


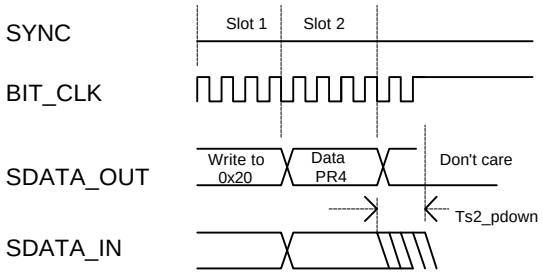
Table 23: Signal Rise and Fall Times

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK rise time	Triseclk	2	-	6	ns
BIT_CLK fall time	Tfallclk	2	-	6	ns
SDATA_IN rise time	Trisedin	2	-	6	ns
SDATA_IN fall time	Tfalldin	2	-	6	ns

7.6 AC-link Low Power Mode Timing

BIT_CLK Stops high in violation of the AC97 specification as noted on the STAC9704/07 errata, but this condition has not caused any known customer problems.

Figure 19: AC-link Low Power Mode Timing



Note: BIT_CLK not to scale

Table 24: AC-link Low Power Mode Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	14	15	us

7.7 ATE Test Mode

Figure 20: ATE Test Mode

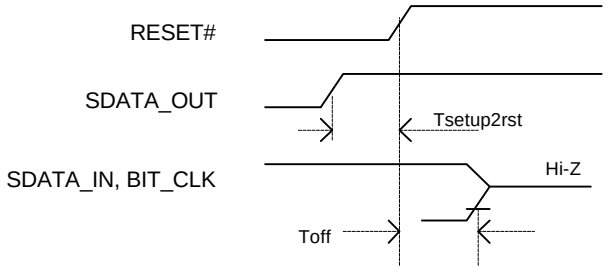


Table 25: ATE Test Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Notes:

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes **STAC9704/7**'s AC-link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once either of the two test modes have been entered, the **STAC9704/7** must be issued another RESET# with all AC-link signals low to return to the normal operating mode.

 # denotes active low.

8. ELECTRICAL SPECIFICATIONS:

8.1 Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0^{o} C TO 70^{o} C
Storage Temperature	-55^{o} C TO $+125^{o}$ C
Soldering Temperature	260^{o} C FOR 10 SECONDS
Output Current per Pin	± 4 mA except Vrefout = ± 5mA

8.2 Recommended Operating Conditions

Table 26. Operating Conditions

PARAMETER		MIN	TYP	MAX	UNITS
Power Supplies	+ 3.3V Digital	3.135	3.3	3.435	V
	+ 5V Digital	4.75	5	5.25	V
	+ 5V Analog	4.75	5	5.25	V
	+ 3.3V Analog	3.135	3.3	3.435	V
Ambient Temperature		0	-	70	^{o}C

SigmaTel reserves the right to change specifications without notice.

8.3 Power Consumption

Table 27. Power Consumption

PARAMETER		MIN	TYP	MAX	UNITS
Digital Supply Current	+ 5V Digital		45		mA
	+ 3.3V Digital		4		mA
Analog Supply Current	+ 5V Analog		70		mA
	+ 3.3V Analog		62		mA
Power Down Status in Sequence					
PR0 +5V Analog Supply Current			58		mA
PR1 +5V Analog Supply Current			44		mA
PR2 +5V Analog Supply Current			20		mA
PR3 +5V Analog Supply Current			0.1		mA
PR4 +3.3V Digital Supply Current			0.1		mA
PR4 +5V Digital Supply Current			0.1		mA
PR5 No Effect					

8.4 AC-link Static Digital Specifications ($T_{ambient}$ = 25 ^{o} C, DVdd = 5.0V or 3.3V ±5%, AVss=DVss=0V; 50pF external load)

Table 28. AC-link Static Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	Vin	-0.30		DVdd + 0.30	V
Low level input range	Vil	-	-	0.30xDVdd	V
High level input voltage	Vih	0.40xDVdd	-	-	V
High level output voltage	Voh	0.50xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.2xDVdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4		mA

8.5 STAC9704 Analog Performance Characteristics

($T_{ambient}$ = 25° C, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0dB = 1 Vrms, 10K ohm/ 50pF load, Testbench Characterization BW: 20 Hz – 20kHz, 0dB settings on all gain stages**)**

Table 29. Analog Performance Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:				
Line Output 5V	-	1.0	-	Vrms
Analog S/N:				
CD to LINE_OUT 5V	90	98	-	dB
Other to LINE_OUT 5V	-	98	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A 5V	85	96	-	dB
A/D 5V	75	87	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	–	dB
Out-of-Band Rejection[7]	-	+40	–	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	+40	–	dB
Crosstalk between Input channels	-	-	-70	dB
Spurious Tone Rejection	-	+100	–	dB
Attenuation, Gain Step Size	-	1.5	–	dB
Input Impedance	10	-	–	K Ohm
Input Capacitance	-	15	–	pF

Vrefout	-	0.41 x AVdd	–	V
Interchannel Gain Mismatch ADC			0.5	dB
Interchannel Gain Mismatch DAC		-	0.5	dB
Gain Drift		100		ppm/ ^{o} C
DAC Offset Voltage		10	50	mV
Deviation from Linear Phase			1	degree
External Load Impedance	10			K ohm
Mute Attenuation (Vrms input)	90	96		dB

Notes:

1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

8.6 STAC9707 Analog Performance Characteristics ($T_{ambient}$ = 25° C, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0dB = 1 Vrms, 10K ohm/ 50pF load, Testbench Characterization BW: 20 Hz – 20kHz, 0dB settings on all gain stages)

Table 30. Analog Performance Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Output Voltage:				
Line Inputs to line output 3.3V	-	0.5	-	Vrms
Line Inputs to LINE_OUT 3.3V @ Line In = 1 Vrms and @ Gain setting of -6 dB		0.5		Vrms
Line Inputs to LINE_OUT 3.3V @ Line In = 0.5 Vrms and @ gain setting of 0dB		0.5		Vrms
PCM to LINE_OUT 3.3V @ full scale PCM input @PCM gain setting of 0dB		0.5		Vrms
PCM to Line Output 3.3V				
MIC Inputs to LINE_OUT 3.3V @ MIC In = 1 Vrms and @ gain setting of 0dB		0.5		Vrms
Analog S/N:				
CD to LINE_OUT 3.3V	-	90	-	
Other to LINE_OUT 3.3V		90		
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A 3.3V	85	90	-	
A/D 3.3V	75	85	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	–	dB
Out-of-Band Rejection[7]	-	+40	–	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	+40	–	dB
Crosstalk between Input channels	-	-	-70	dB

Spurious Tone Rejection	-	+100	–	dB
Attenuation, Gain Step Size	-	1.5	–	dB
Input Impedance	10	-	–	K Ohm
Input Capacitance	-	15	–	pF
Vrefout	-	0.41 x AVdd	–	V
Interchannel Gain Mismatch ADC			0.5	dB
Interchannel Gain Mismatch DAC		-	0.5	dB
Gain Drift		100		ppm/ ^{o} C
DAC Offset Voltage		10	50	mV
Deviation from Linear Phase			1	degree
External Load Impedance	10			K ohm
Mute Attenuation (0 dB)	90	96		dB

Notes:

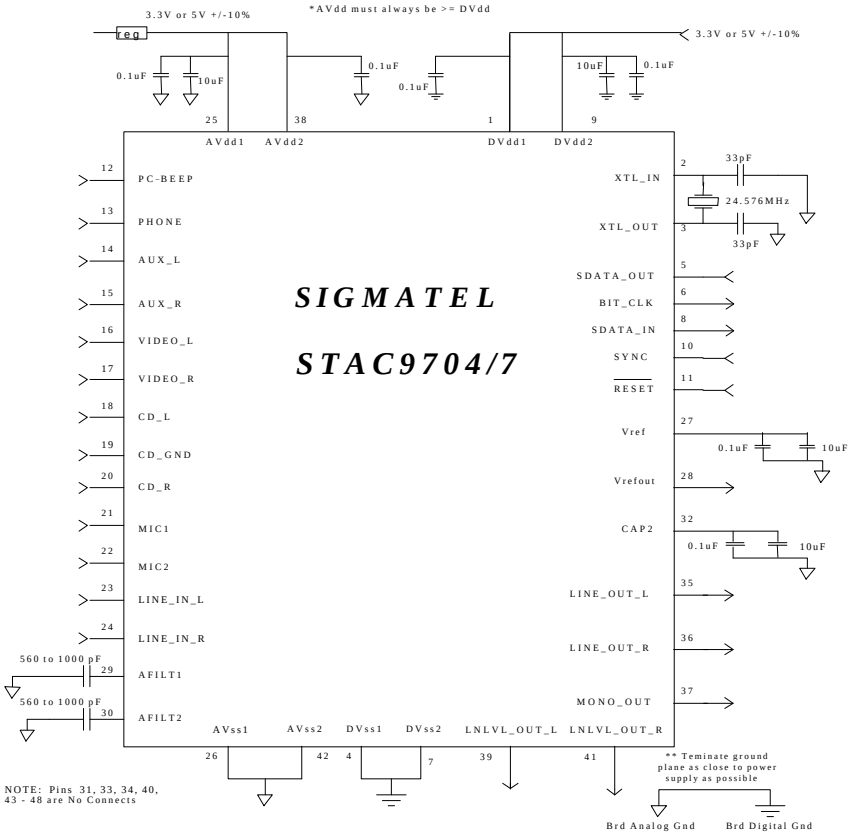
1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

Appendix A

SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the STAC9704/7 may be derived from a supply regulator (as shown in Figure 3) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's codecs would be subject to on-chip SCR type latch-up.

SigmaTel's STAC9704/7 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.



Appendix B

+5.0V/+3.3V POWER SUPPLY OPERATION NOTES

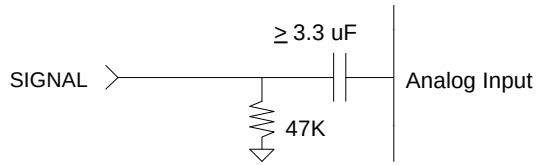
The STAC9704 is capable of operating from a single 5V supply connected to both DVdd and AVdd. Even though the STAC9704 has digital switching levels of 0.2Vdd to 0.5Vdd (See AC Link Electrical Characteristics in this data book), we recommend that all digital interface signals to the AC-Link be 5V. If digital interface signals below 5V are used, then appropriate level shifting circuitry must be provided to ensure adequate digital noise immunity.

The STAC9704 can also operate from a 3.3V digital supply connected to DVdd while maintaining a 5V analog supply on AVdd. On-chip level shifters ensure accurate logic transfers between the analog and digital portions of the STAC9704. If digital interface signals above 3.3V are used (i.e. a +5V AC-Link interface), then appropriate level shifting circuitry must be provided to ensure adequate digital noise immunity and to prevent on-chip ESD protection diodes from turning on. (See Appendixes A concerning SPLIT INDEPENDENT POWER SUPPLY OPERATION).

The STAC9707 must be run from a 3.3V supply connected to both DVdd and AVdd. If digital interface signals above 3.3V are used (i.e. a +5V AC-Link interface), then appropriate level shifting circuitry must be provided to ensure adequate digital noise immunity and to prevent on-ship ESD protection diodes from turning on.

***Always operate the STAC97xx digital supply from the same supply voltage as the digital controller supply.**

***All the analog inputs must be ac-coupled with a capacitor of 3.3 uF or greater. It is recommended that a resistor of about 47k ohm be connected from the signal side of the capacitor to analog GND as shown below.**



***All the analog outputs must be ac-coupled. If an external amplifier is used, make sure that the input impedance of the amplifier is at least 10K ohm and use an ac-coupling capacitor of 3.3 uF.**

- NOTES -

- NOTE -

For more information, please contact:

SigmaTel, Inc.
6101 W. Courtyard Dr., Bldg. 1, Suite 100
Austin, Texas 78730
Tel (512) 343-6636, Fax (512) 343-6199
email: sales@sigmatel.com
Homepage: www.sigmatel.com